UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,326	07/03/2003	Daniel M. Kinzer	IR-2541 DIV	4283

2352 7590 05/05/2004

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,326	KINZER ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 27 is objected to because of the following informalities: There is no antecedent basis for the claimed limitation "said first plurality of diffusions" as claimed in claim 27. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2, 6-7, 9-11 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, in lines 3-4 (or claim 13, in lines 3-4), the phrase "said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgate device" fails to clarify the claimed invention, in which the first, second, bottom and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgate device.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,578,841 to Vasquez et al.

Regarding claim 1, Vasquez et al. (figure 1) teach a flip chip semiconductor device comprising a silicon wafer (34) having parallel first (an upper surface of the wafer [34])) and second (a bottom surface of the wafer [34])) major surfaces; at least one P region (P region in the epitaxial [17]) and at least one N region (N region in the channel [14]) in the wafer which meet at a PN junction within the silicon wafer (34); first (21 is located on the left side of figure 1) and second (21 is located on the right side of figure 1) are coplanar, laterally spaced and metallized layers (left [21], right [21]) formed on the first (an upper surface of the wafer [34]) major surface and insulated form one another and connected to the P region and the N region respectively; and a bottom metallized layer (26) extending across the second major surface (a bottom surface of the wafer [34]).

Regarding claim 2, Vasquez et al. teach a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced from the first (left [21]) and second (right [21]) metallized layers; the first, second and third metallized layers comprising source and gate electrodes respectively of a MOS gated device.

Regarding claims 3-4, Vasquez et al. teach at least one contact bump (24) connected to each of the metallized layers (left [21], 23 and right [21]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,578,841 to Vasquez et al.

Regarding claims 5-7, Vasquez et al. differ from the claimed invention by not showing the bottom metallized layer is substantially thicker than all of the first and second metallized layers. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the bottom metallized layer is substantially thicker than all of the first and second metallized layers because it improves the thermal conduction of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claim 8, Vasquez et al. differ from the claimed invention by not showing the bottom metallized layer is substantially thicker than all of the first and second metallized layers. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the bottom metallized layer is substantially thicker than all of the first and second metallized layers because it improves the thermal conduction of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable of a result effective

variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claims 9-10, Vasquez et al. teach a plurality of contact bumps (24) is connected to each of the first (left [21]) and second (right [21]) metallized layers.

Vasquez et al. differ from the claimed invention by not showing the plurality of contact bumps connected to the first metallized layer being aligned along a first straight row and the plurality of contact bumps connected to the second metallized layer being aligned along a second straight row and the first and second rows are parallel to one another. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the plurality of contact bumps connected to the first metallized layer being aligned along a first straight row and the plurality of contact bumps connected to the second metallized layer being aligned along a second straight row because it provides interconnection between the chip and the external device.

Regarding claim 11, Vasquez et al. teach a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced from the first (left [21]) and second (right [21]) metallized layers; the first, second and third metallized layers comprising source and gate electrodes respectively of a MOS gated device.

Regarding claims 12 and 16, Vasquez et al. (figure 1) teach a flip chip semiconductor device comprising a silicon wafer (34) having parallel first (an upper surface of the wafer [34])) and second (a bottom surface of the wafer [34])) major surfaces; at least one P region (P region in the epitaxial [17]) and at least one N region (N region in the channel [14]) in the wafer which meet at a PN junction within the silicon wafer (34); first (21 is located on the left side of figure

1) and second (21 is located on the right side of figure 1) are coplanar, laterally spaced and metallized layers (left [21], right [21]) formed on the first (an upper surface of the wafer [34]) major surface and insulated form one another and connected to the P region and the N region respectively; and a plurality of contact bumps (24) connected to each of the first (left [21]) and second (right [21]) metallized layers.

Vasquez et al. differ from the claimed invention by not showing the plurality of contact bumps connected to the first metallized layer being aligned along a first straight row and the plurality of contact bumps connected to the second metallized layer being aligned along a second straight row and the first and second rows are parallel to one another. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the plurality of contact bumps connected to the first metallized layer being aligned along a first straight row and the plurality of contact bumps connected to the second metallized layer being aligned along a second straight row because it provides interconnection between the chip and the external device.

Regarding claim 13, Vasquez et al. teach a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced from the first (left [21]) and second (right [21]) metallized layers; the first, second and third metallized layers comprising source and gate electrodes respectively of a MOS gated device.

Regarding claim 14, Vasquez et al. teach a bottom metallized layer (26) extending across the second major surface (a bottom surface of the wafer [34]).

Regarding claim 15, Vasquez et al. differ from the claimed invention by not showing the bottom metallized layer is substantially thicker than all of the first and second metallized layers.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the bottom metallized layer is substantially thicker than all of the first and second metallized layers because it improves the thermal conduction of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claims 17 and 19, Vasquez et al. teach silicon wafer is a rectangular wafer having an area defined by a given length and a given width, the length being greater than the width.

Vasquez et al. differ from the claimed invention by not showing the first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across the wafer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across the wafer because it provides interconnection between the chip and the external device.

Regarding claim 18, Vasquez et al. teach a third metallized layer (23) atop the first (an upper surface of the wafer [34]) major surface which is coplanar with and laterally spaced from the first (left [21]) and second (right [21]) metallized layers; the first, second and third metallized layers comprising source and gate electrodes respectively of a MOS gated device.

Regarding claim 20, Vasquez et al. teach a bottom metallized layer (26) extending across the second major surface (a bottom surface of the wafer [34]).

7. Claims 21, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,574,208 to Lade et al. in view of US Patent No. 6,489,678 to Joshi.

Regarding claim 21, Lade et al. (figures 12-16) teach a bi-directional conduction device comprising a silicon wafer having first (an upper surface of the wafer [104]) and second (a bottom surface of the wafer [104]) parallel major surfaces; first and second laterally separated MOS gated devices formed in the silicon wafer; the first and second MOS gated devices comprising a first (126) and a second (128) source region respectively of one conductivity formed into a first and second spaced lateral area respectively of the first major surface (an upper surface of the wafer [104]), a first (140) and second (142) channel region respectively of a second conductivity type receiving the first (126) and second (128) source region, a common drain region (150) receiving the first and second channel regions and extending to the second major surface (a bottom surface of the wafer [104]), and a first and second gate structure respectively disposed on the first major surface (an upper surface of the wafer [104]) and operable to invert respective portions of the first (140) and second (142) channel regions to allow conduction from the first (126) and second (128) source regions respectively to the drain region (150); first (144) and second (146) laterally spaced source metallized layers disposed atop the first (an upper surface of the wafer [104]) major surface and connected to the first (126) and second (128) source regions respectively; and first (144) and second (146) laterally spaced gate metallized layers atop the first major surface (an upper surface of the wafer [104]) and connected to the first and second gate structures respectively.

Lade et al. differ from the claimed invention by not showing flip chip semiconductor device. However, Joshi teaches flip chip semiconductor device package, which is fabricated

using MOSFETs (column 5, lines 38-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Joshi into the device taught by Lade et al. because it provides operating power sources for the chip.

Regarding claim 24, the combined device shows first and second source regions are disposed in laterally interdigitated relation with respect to one another (Lade et al.; figures 14-16; column 10, line 11 – column 12, line 43).

Regarding claim 26, the combined device differs from the claimed invention by not showing a metal layer on the second major surface in the embodiment of figures 12-16. However, Lade et al. teach a metal layer on the second major surface in the embodiment of figure 1. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include claimed limitation shown in the embodiment of figure 1 into the embodiment of figures 12-16 because it provides interconnection from the bottom surface of the substrate to the external device. The combined device shows a metal layer on the second major surface.

8. Claims 22, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lade et al. in view of Joshi, and further in view of US Patent No. 5,352,926 to Andrews.

Regarding claim 22, the disclosures of Lade et al. and Joshi are discussed as applied to claim 21 above.

The combined device differs from the claimed invention by not showing at least one contact bump connected to each of the metallized layers. However, Andrews (figures 1-2) teaches at least one contact bump connected to each of the source and gate (column 3, lines 19-

25). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Andrews into the device taught by Lade et al. and Joshi because it provides interconnection between the semiconductor chip and external device. The combined device shows at least one contact bump connected to each of the source and gate metallized layers.

Regarding claim 23, the combined device shows a respective plurality of contact bumps (Andrews; 32) connected to each of the source metallized layers; each of the plurality of contact bumps (Andrews; 34) arranged in respective spaced rows which are parallel to one another.

Regarding claim 25, the combined device shows first and second source regions are disposed in laterally interdigitated relation with respect to one another (Lade et al.; figures 14-16; column 10, line 11 – column 12, line 43).

9. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,321,289 to Baba et al. in view of US Patent No. 5,578,841 to Vasquez et al. and US Patent No. 4,574,208 to Lade et al.

Regarding claim 27, Baba et al. (figures 1A-B) teach a semiconductor device comprising a silicon die having first (an upper surface of the substrate [10, 11, 12]) and second (a bottom surface of the substrate [10, 11, 12]) parallel surfaces; a region of one conductivity type (diffusion region of [13]) extending from the first surface (an upper surface of the substrate [10, 11, 12]) and into the body of the die; a junction pattern defined in the device formed by a plurality of laterally spaced diffusions (diffusion region of [12]) of the other conductivity type into the region of one conductivity type; a first conductive electrode (left S) formed atop the first

surface (an upper surface of the substrate [10, 11, 12]) and in contact with the plurality of diffusions (diffusion regions of [12], [13]); a second conductive electrode (right S) formed atop the first surface (an upper surface of the substrate [10, 11, 12]) which is coplanar with and laterally spaced from and insulated from the first conductive electrode (left S) and in electrical contact with the body of the die through a high conductivity element.

Baba et al. differ from the claimed invention by not showing at least one solder ball connector formed atop each of the first and second conductive electrodes respectively. However, Vasquez et al. (figure1) teach forming at least one solder ball (24) connector atop each of the first (left [21]) and second (right [21]) conductive electrodes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Vasquez et al. into the device taught by Baba et al. because it provides interconnection between the semiconductor device and the external device. The combined device shows at least one solder ball connector formed atop each of the first and second conductive electrodes respectively.

Baba et al. and Vasquez et al. further differ from the claimed invention by not showing the current path from the first conductive electrode to the second conductive electrode having a vertical component, which is generally perpendicular to the first surface. However, Lade et al. teach the orientation of current flow in vertical (column 3, lines 1-13). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lade et al. into the device taught by Baba et al. and Vasquez et al. because it improves the electrical performance of the device. The combined device shows the

current path from the first conductive electrode to the second conductive electrode having a vertical component, which is generally perpendicular to the first surface.

Regarding claim 28, the combined device shows high conductivity element is a sinker diffusion of higher conductivity than the body region.

Regarding claim 29, the combined device shows high conductivity element is a metallic material residing in a trench formed in the body of the die.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
April 29, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800